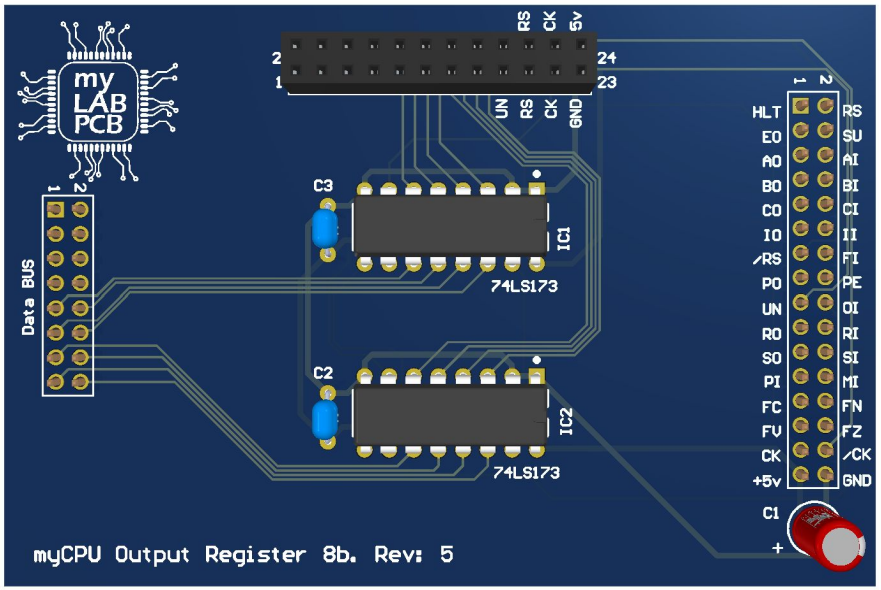
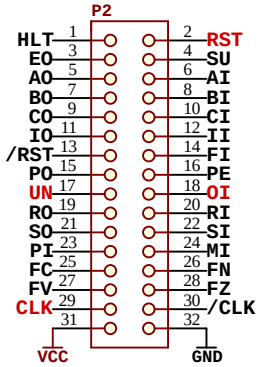
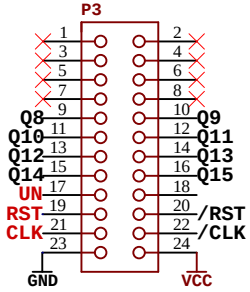

my
LAB
PCB
RS
CK
5v
2
1
24
23
UN
RS
CK
GND
1
2
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
C3
IC1
74LS173
C2
IC2
74LS173
C1
+
myCPU Output Register 8b. Rev: 5

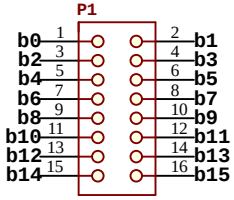
Control BUS Connector



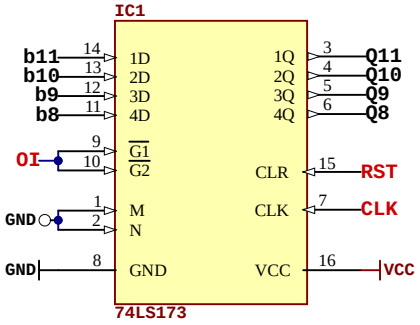
OUTPUT Connector

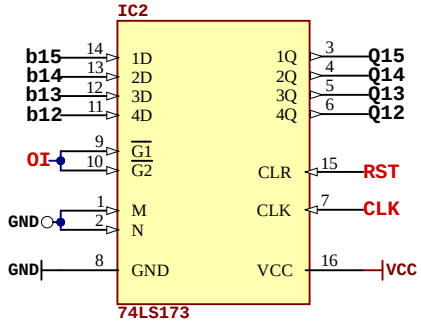


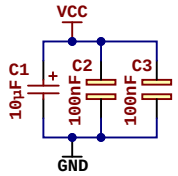
Data BUS Connector



G1, G2 input control.
Set both to LOW using
the OI control signal
to load all input bits
into flip-flops

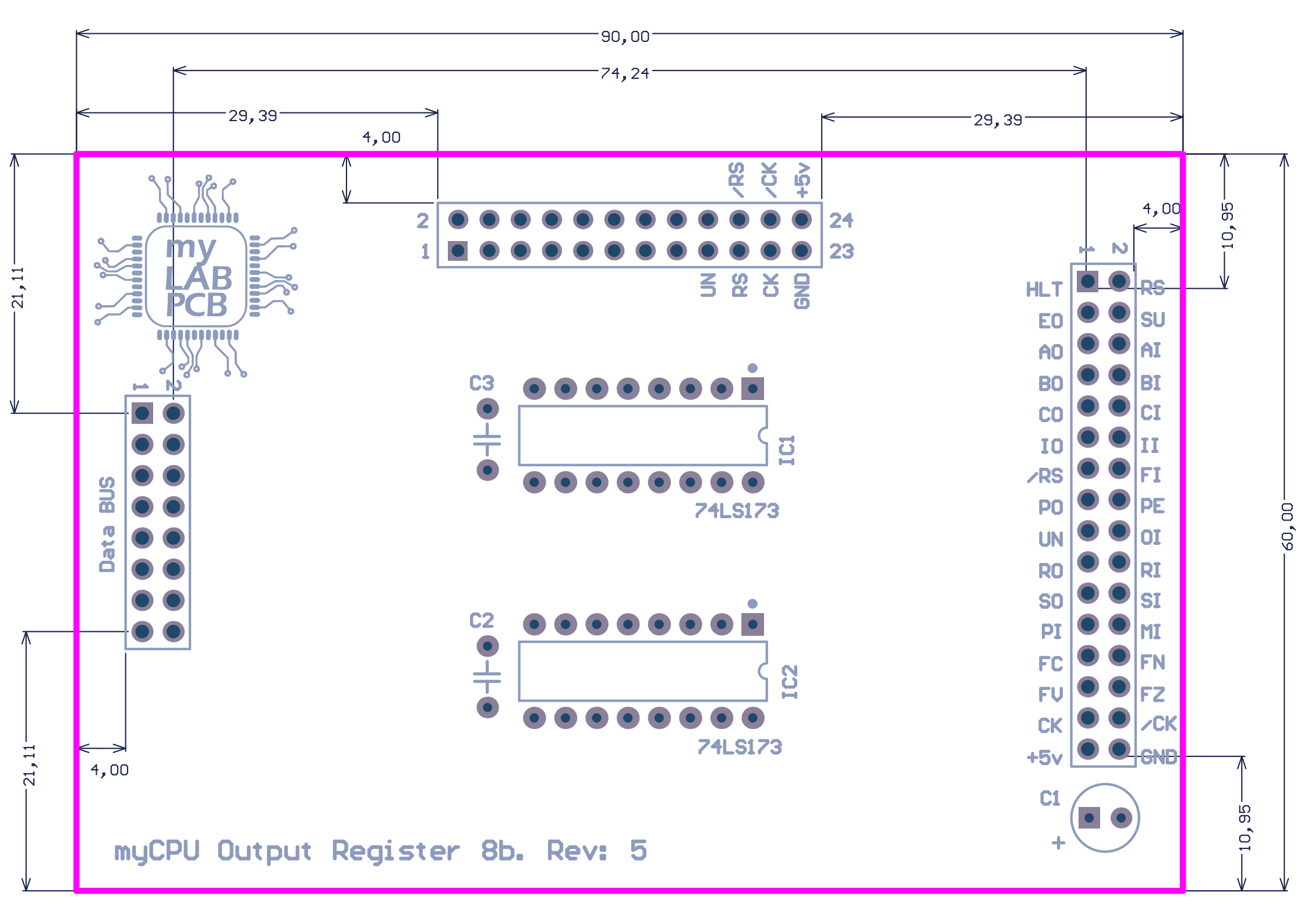


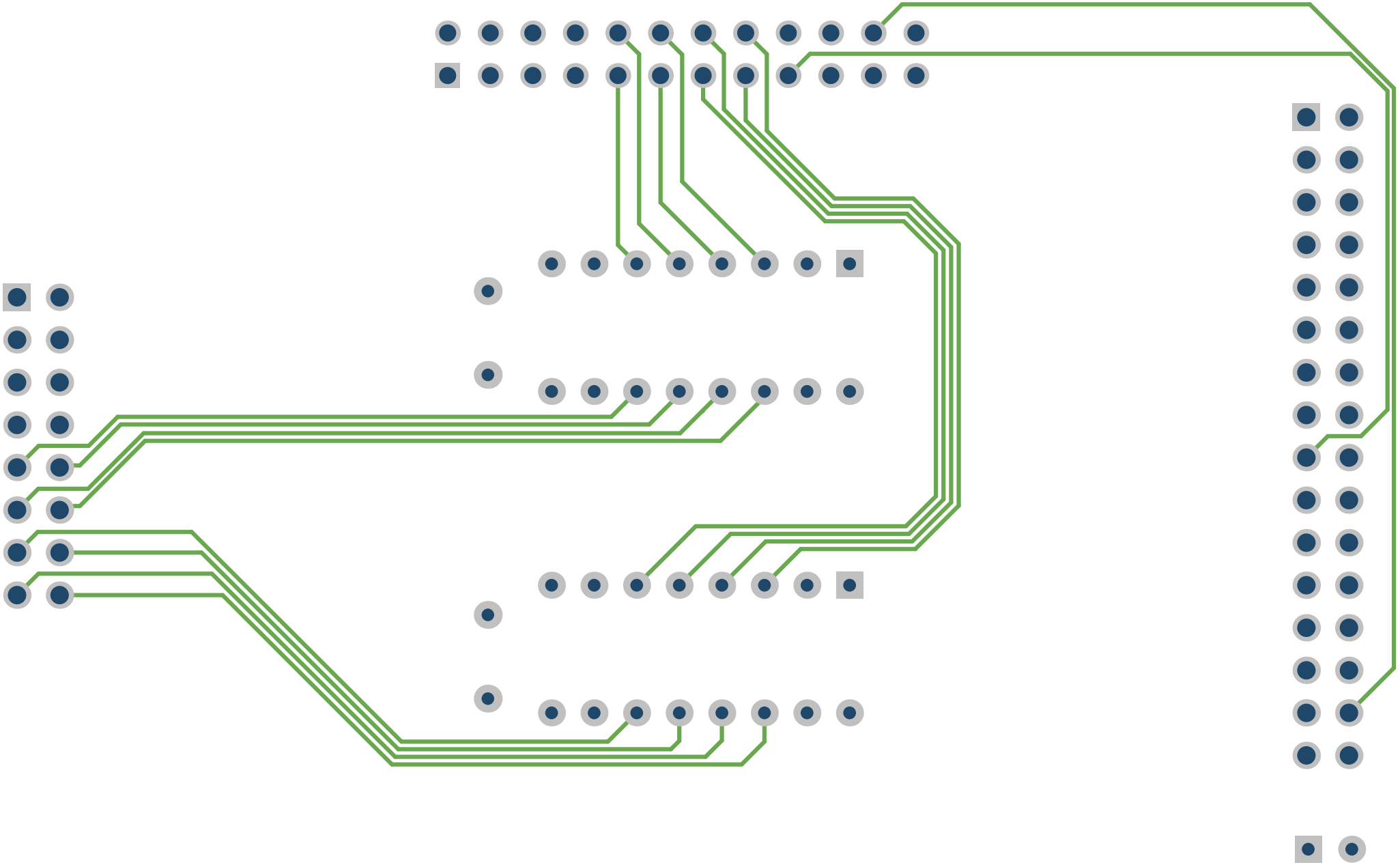


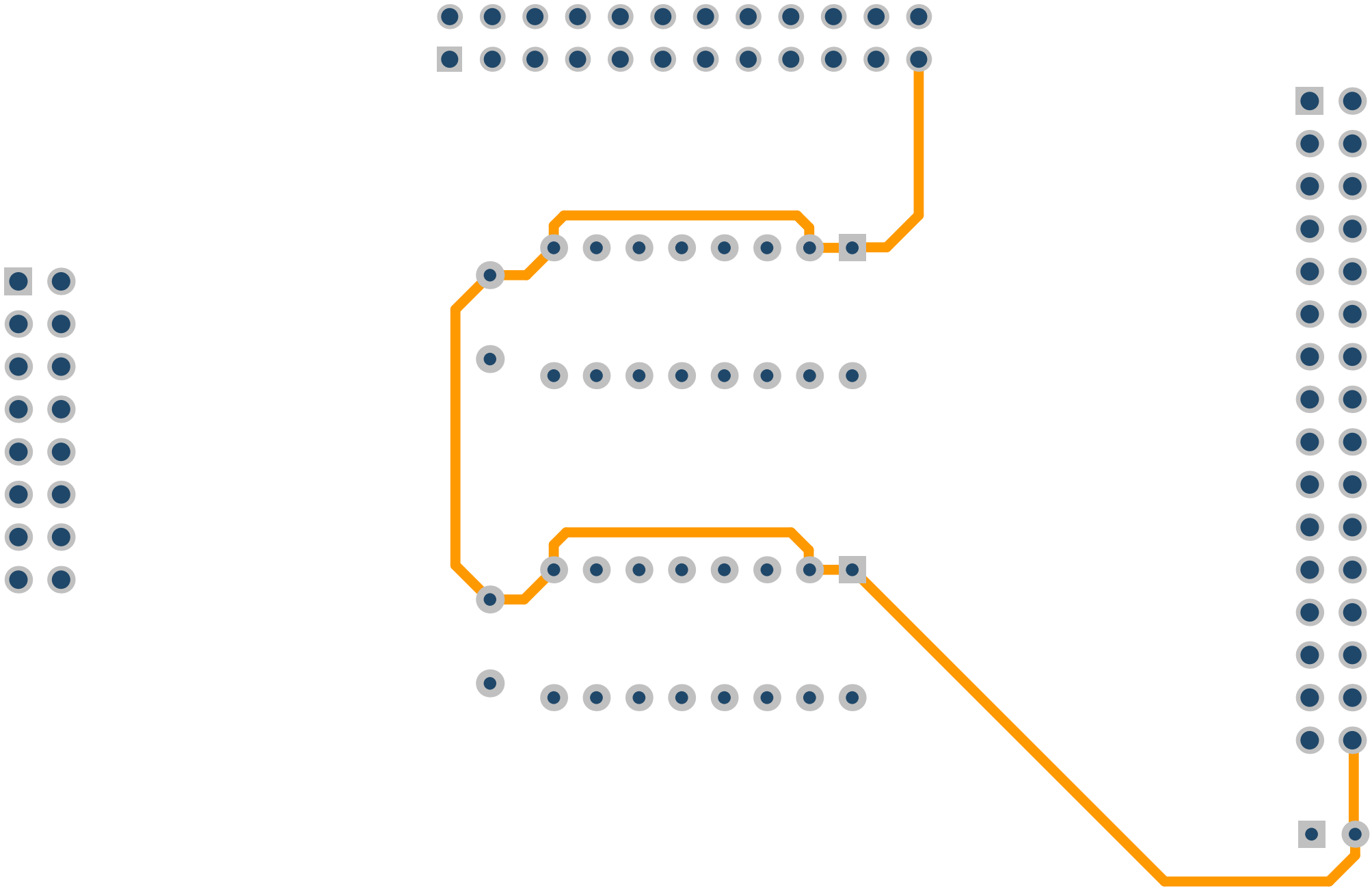


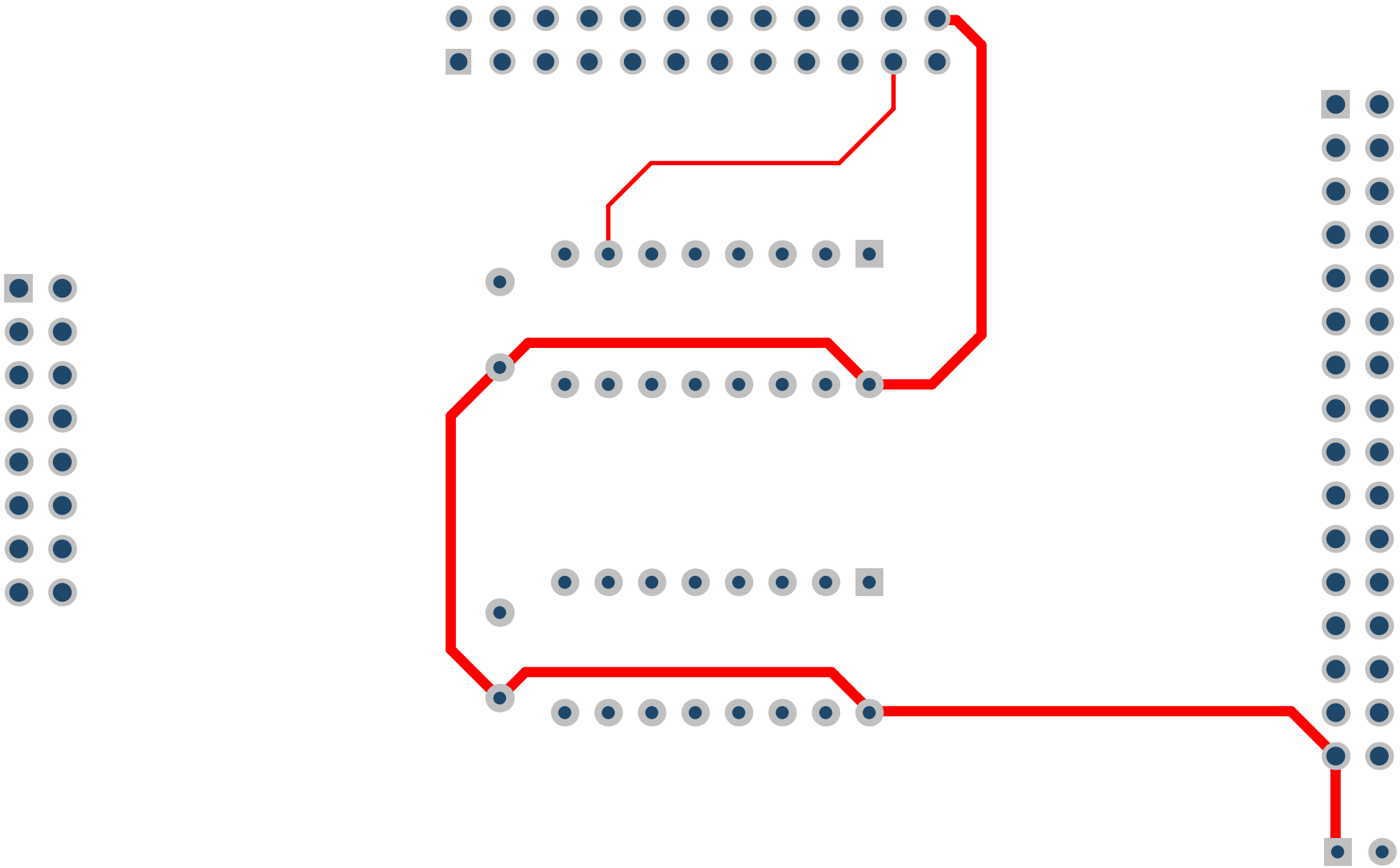
Decoupling Capacitors

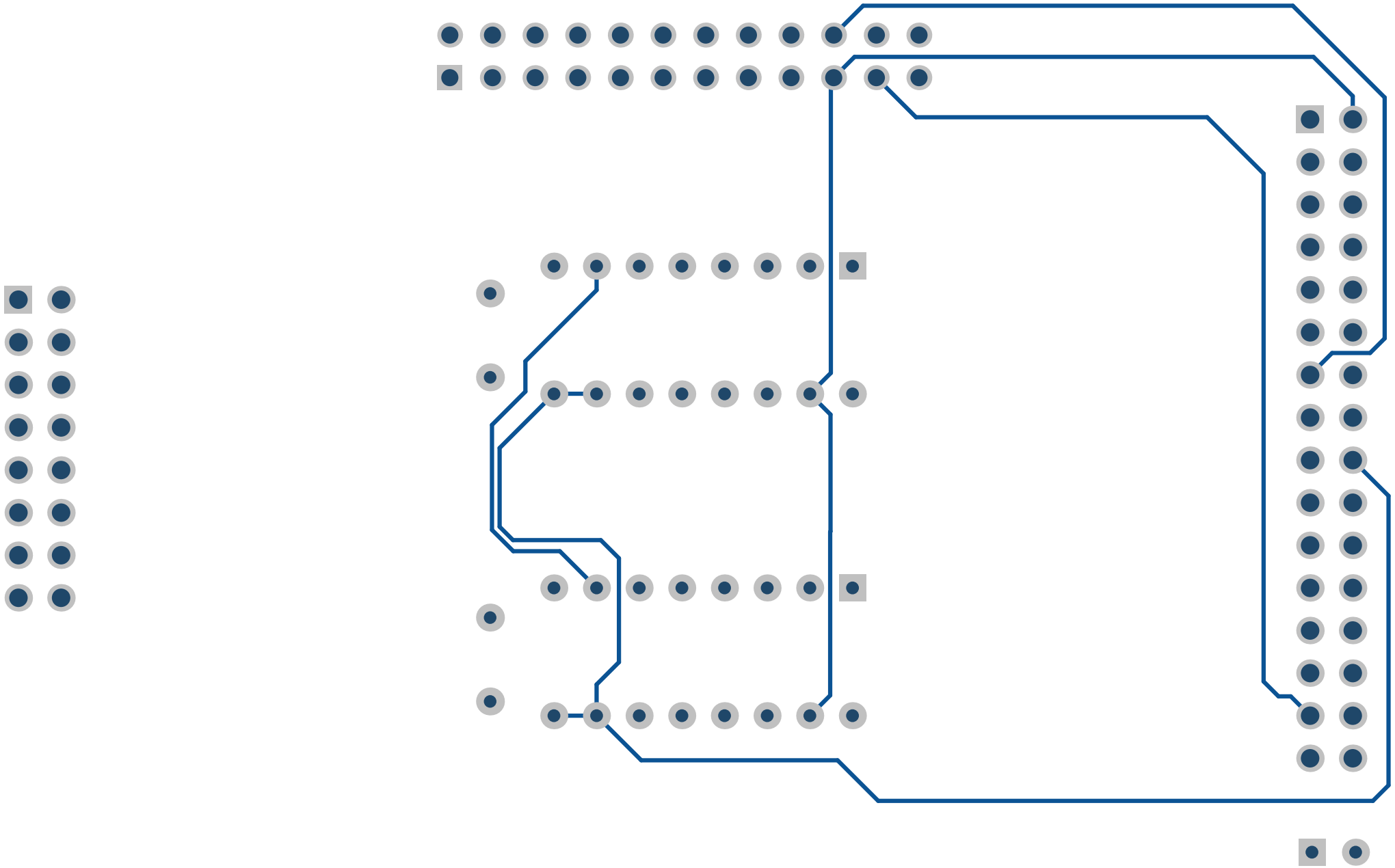
Project: myCPU Output Register 8 bit	
Revision: 5	**Date:** 13/03/2023
Author: Rafa Hernández	


90,00
74,24
29,39
4,00
29,39
21,11
/RS
/CK
+5v
2
1
24
23
UN
RS
CK
GND
4,00
10,95
60,00
my
LAB
PCB
1
2
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
C3
IC1
74LS173
C2
IC2
74LS173
C1
+
21,11
4,00
10,95
myCPU Output Register 8b. Rev: 5









Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C2, C3	Ceramic or tantalum capacitor	100nF	2
IC1, IC2	4-bit D-Type Register with 3 state outputs	74LS173	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1

Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
IC1	4-bit D-Type Register with 3 state outputs	74LS173
IC2	4-bit D-Type Register with 3 state outputs	74LS173
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p